CLAIMS:

1. A method for configuring a routing program for routing connections between an integrated circuit device and an embedded core, comprising:

obtaining a first horizontal pitch and a first vertical pitch for one of the integrated circuit device and the embedded core;

obtaining a second horizontal pitch and a second vertical pitch for the other of the integrated circuit device and the embedded core, the first vertical pitch and the second vertical pitch being different;

inputting a first connection layer input to the routing program, the first connection layer input including the first vertical pitch and a horizontal direction; and

inputting a second connection layer input to the routing program, the second connection layer input including the second horizontal pitch and a vertical direction.

2. The method of Claim 1 wherein the one of the integrated circuit device and the embedded core is a programmable logic device.

3. The method of Claim 2 wherein the other of the integrated circuit device and the embedded core is a microprocessor core.

4. The method of Claim 3 wherein the programmable logic device is a field programmable gate array.

5. The method of Claim 4 wherein the field programmable gate array and the microprocessor core are formed as separate integrated circuits which are interconnected, the field programmable gate array having a first plurality of metal

layers, the microprocessor core having a second plurality of metal layers, at least one layer of the first plurality of metal layers having the first horizontal pitch and the first vertical pitch, and at least one layer of the second plurality of metal layers having the second horizontal pitch and the second vertical pitch.

6. A method for configuring a routing program for routing to an integrated circuit device having an embedded core, comprising:

providing a first horizontal pitch and a first vertical pitch for one of the integrated circuit device and the embedded core;

providing a second horizontal pitch and a second vertical pitch for the other of the integrated circuit device and the embedded core, the first horizontal pitch and the second horizontal pitch being different;

inputting a first connection layer input to the routing program, the first connection layer input including the first horizontal pitch and a vertical direction; and

inputting a second connection layer input to the routing program, the second connection layer input including the second vertical pitch and a horizontal direction.

7. The method of Claim 6 wherein the one of the integrated circuit device and the embedded core is a programmable logic device.

8. The method of Claim 7 wherein the other of the integrated circuit device and the embedded core is a microprocessor core.

9. The method of Claim 8 wherein the programmable logic device is a field programmable gate array.

10. The method of Claim 9 wherein the field programmable gate array and the microprocessor core are formed as separate integrated circuits which are interconnected, the field programmable gate array having a first plurality of metal layers, the microprocessor core having a second plurality of metal layers, at least one layer of the first plurality of metal layers having the first horizontal pitch and the first vertical pitch, and at least one layer of the second plurality of metal layers having the second horizontal pitch and the second vertical pitch.

11. An integrated circuit device, comprising:

a first device coupled to a second device;

the first device comprising a first horizontal pitch and a first vertical pitch;

the second device comprising a second horizontal pitch and a second vertical pitch; and

at least one interconnect layer for coupling the first device and the second device, the interconnect layer comprising a set of pitches selected from:

(i) the first vertical pitch and the second horizontal pitch; and

(ii) the first horizontal pitch and the second vertical pitch.

12. The integrated circuit device of Claim 11 further comprising a plurality of logic blocks for interconnecting the first device and the second device.

13. The integrated circuit of Claim 12 wherein the first device is a programmable logic device.

14. The integrated circuit of Claim 13 wherein the programmable logic device is a field programmable gate array.

15. The integrated circuit of Claim 13 wherein the second device is a microprocessor core.

16. The integrated circuit of Claim 15 wherein the microprocessor core is embedded in the programmable logic device.

17. The integrated circuit of Claim 16 wherein the programmable logic device comprises more metal interconnect layers than the microprocessor core.

18. The integrated circuit of Claim 11 wherein the second device comprises a plurality of pins for interconnection thereto.

19. The integrated circuit of Claim 11 wherein the interconnect layer was routed using a routing program having as inputs the set of pitches.

20. The integrated circuit of Claim 19 wherein the set of pitches is divided for input to the routing program, wherein one pitch in the set of pitches is for one metal layer and the other pitch in the set of pitches is for another metal layer.